BILASPUR UNIVERSITY

YEAR 2016-17

A PROJECT REPORT ON
VERIFICATION UNIVERSAL GATES

SUBMITTED IN THE PARTIAL FULFILLMENT OF
REQUREMENT FOR THE DEGREE OF THE MASTER OF SCINCE
IN FHYSICS UNDER THE BILASPUR UNIVERSITY (C.G.)

Guided by
Dr. K.K. Dubey
Asst. Professor
Dept.of Physics

Submitted by
MADHURI PATEL
M.Sc. Physics (Final)
Enrollment No BUS/ 12/622/1094

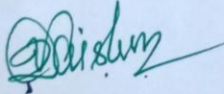**DIPARTMENT OF PHYSICS**
GOVT. COLLEGE HARDI BAZAR
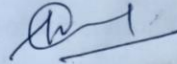**DIST. KORBA (C.G.)**

Certificate

This is certify that **MADHURI PATEL** has completed his project entitled "VERIFICATION OF **Universal Gates** and are submitting that for the degree of M.Sc. Final Physics. The above referred project is duly completed an up to the standard, both in respect of its literacy presentation, for being referred to the examiner. I further certify that the work contained in his project has been done by.

Thereby forward his project report for award M.Sc. Final Physics, Govt. College Hardibazar, Dist. Korba (C.G.)
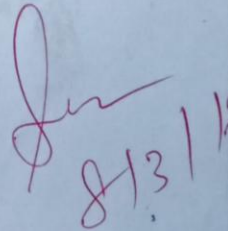
Date :.........................

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8/3/1

Dr. Kartikeshwar Dubey

Asst. Professor
Department of Physics

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Date :....................

Certificate

This is certify that MADHURI PATEL has carriedout the work on the project of "VERIFICATION OF DE Universal Gates under my supervision during the session 2016-17 in partial fulfillment of the course prescribed of the degree of Master of Science in Physics.
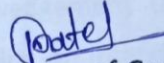
Signature of Supervisor

(Dr. K. K. Dubey)
Asst. Professor
Department of Physics
Govt. College Hardibazar
Dist. Korba (C.G.)

Declaration

I hereby declare that the project report entitled " **VERIFICATION OF Universal Gates** submitted by me during the session 2016-17 under the supervision of **Dr. K. K. Dubey**, Asst. Professor of Physics, Govt. College Hardibazar, KORBA (C.G.)

Date : 8/3./2017.

Place :.....................

Signature of Candidate

MADHURI PATEL

Acknowledgement

I express my deep sense of gratitudfe and heartfelt thank to **Dr. T. D. Vaishnav**, Principal of Govt. College Hardibazar, Korba (C.G.)

I express my deep sense of gratitudfe and heartfelt thank to **Dr. K.K. Dubey**, H.O.D. of Physics in his in estimate guidance and keen interest in development of this work.

It is greatest pleasure to acknowedgement the generous encouragement and source of inspiration intended to me by **Dr. K.K. Dubey** Asst. Professor.

I am very greatful to Mr. **Lalji Sahu**, lab technician of physics and **Mr. A. K. Upadh**yay for their help at various stage during my project work.

I am very thankfully to my "Parents" and "Sister" for their blessing and encouragement to do this.

Date : ....

Place :...................

**Signature of Candidate**

MADHURI PATEL

NOR Gate:

The **NOR** gate represents the complement of the OR operation. Its name is an abbreviation of **NOT OR**.

The graphic symbol for the NOR gate consists of an OR symbol with a bubble on the output, denoting that a complement operation is performed on the output of the OR gate.

The truth table and the graphic symbol of NOR gate is shown in the figure.

X	Y	NOR
0	0	1
0	1	0
1	0	0
1	1	0

$$Z = \overline{X + Y}$$
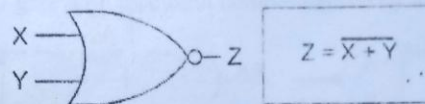
The truth table clearly shows that the NOR operation is the complement of the OR.

Universal Gates:

A universal gate is a gate which can implement any Boolean function without need to use any other gate type.

The NAND and NOR gates are universal gates.

In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

In fact, an AND gate is typically implemented as a NAND gate followed by an inverter not the other way around!!

Likewise, an OR gate is typically implemented as a NOR gate followed by an inverter not the other way around!!

NAND Gate is a Universal Gate:

To prove that any Boolean function can be implemented using only NAND gates, we will show that the AND, OR, and NOT operations can be performed using only these gates.
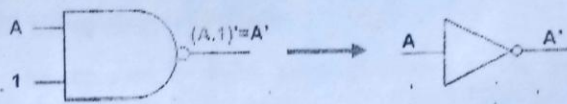
Implementing an Inverter Using only NAND Gate

The figure shows two ways in which a NAND gate can be used as **an inverter (NOT gate)**.

1. All NAND input pins connect to the input signal A gives an output A'.
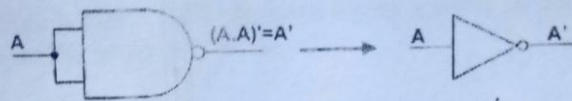
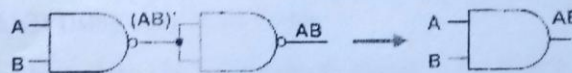2. One NAND input pin is connected to the input signal A while all other input pins are connected to logic 1. The output will be A'.

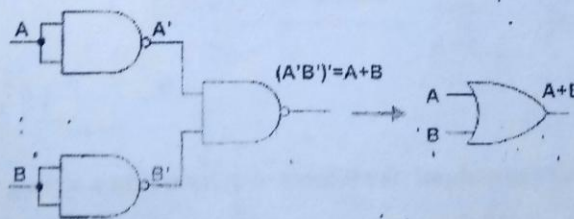

Implementing AND Using only NAND Gates

An AND gate can be replaced by NAND gates as shown in the figure (The AND is replaced by a NAND gate with its output complemented by a NAND gate inverter).

Implementing OR Using only NAND Gates

An OR gate can be replaced by NAND gates as shown in the figure (The OR gate is replaced by a NAND gate with all its inputs complemented by NAND gate inverters).

Thus, the NAND gate is a universal gate since it can implement the AND, OR and NOT functions.

## NAND Gate is a Universal Gate:

To prove that any Boolean function can be implemented using only NOR gates, we will show that the AND, OR, and NOT operations can be performed using only these gates.
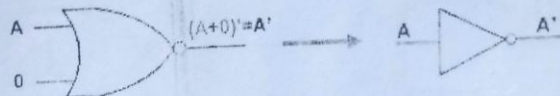
Implementing an Inverter Using only NOR Gate

The figure shows two ways in which a NOR gate can be used as **an inverter (NOT gate)**.

**1. All NOR input pins connect to the input signal A gives an output A'.**

$$(A+A)'=A' \qquad A \triangleright\!\!\circ\; A'$$
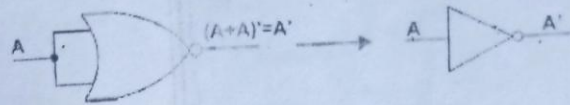
2. One NOR input pin is connected to the input signal A while all other input pins are connected to logic 0. The output will be A'.


$$(A+0)'=A' \qquad A \triangleright\!\!\circ\; A'$$

Implementing OR Using only NOR Gates

An OR gate can be replaced by NOR gates as shown in the figure (The OR is replaced by a NOR gate with its output complemented by a NOR gate inverter)
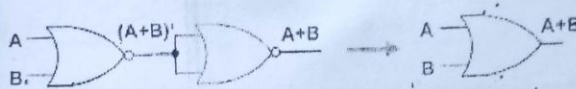
Implementing AND Using only NOR Gates

An AND gate can be replaced by NOR gates as shown in the figure (The AND gate is replaced by a NOR gate with all its inputs complemented by NOR gate inverters)
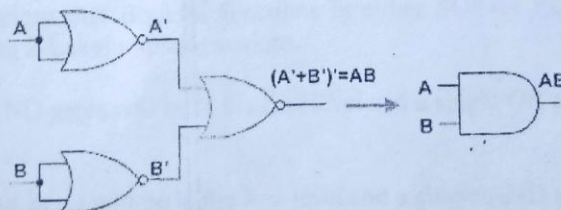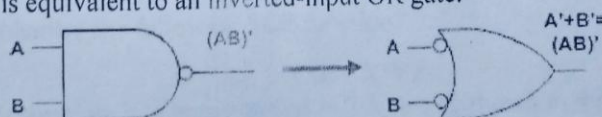

Thus, the NOR gate is a universal gate since it can implement the AND, OR and NOT functions.

Equivalent Gates:

The shown figure summarizes important cases of gate equivalence. Note that bubbles indicate a complement operation (inverter).

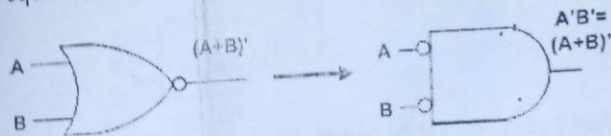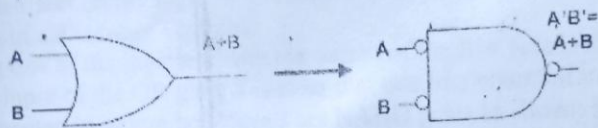A NAND gate is equivalent to an inverted-input OR gate.

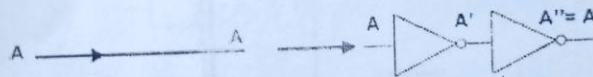An AND gate is equivalent to an inverted-input NOR gate.

A NOR gate is equivalent to an inverted-input AND gate.

An OR gate is equivalent to an inverted-input NAND gate.

Two NOT gates in series are same as a buffer because they cancel each other as $A'' = A$.

Two-Level Implementations:

We have seen before that Boolean functions in either SOP or POS forms can be implemented using 2-Level implementations.

For SOP forms AND gates will be in the first level and a single OR gate will be in the second level.

For POS forms OR gates will be in the first level and a single AND gate will be in the second level.

Note that using inverters to complement input variables is not counted as a level.
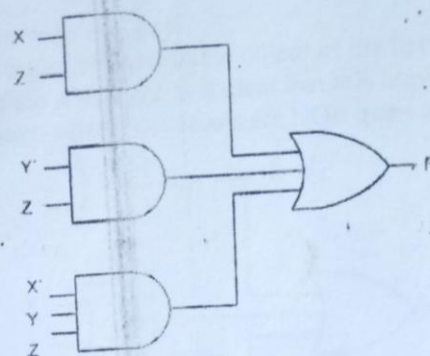
We will show that SOP forms can be implemented using only NAND gates, while POS forms can be implemented using only NOR gates.

This is best explained through examples.
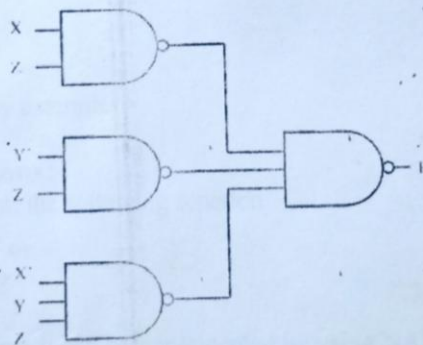
Example 1: Implement the following SOP function

$$F = XZ + Y'Z + X'YZ$$

Being an SOP expression, it is implemented in 2-levels as shown in the figure.

Introducing two successive inverters at the inputs of the OR gate results in the shown equivalent implementation. Since two successive inverters on the same line will not have an overall effect on the logic as it is shown before.

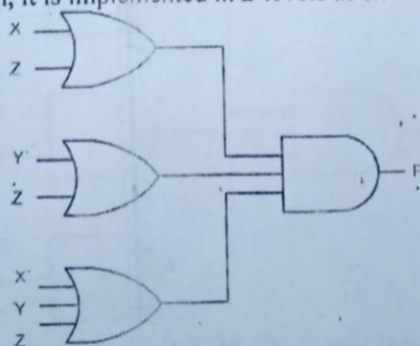(see animation in authorware version)

By associating one of the inverters with the output of the first level AND gate and the other with the input of the OR gate, it is clear that this implementation is reducible to 2-level implementation where both levels are NAND gates as shown in Figure.

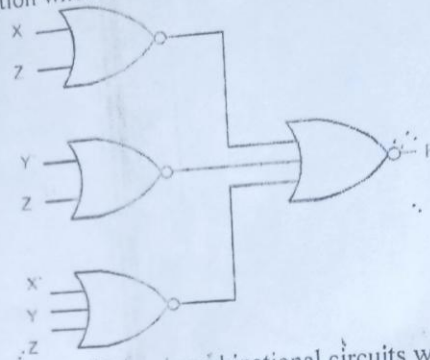
Example 2: Implement the following POS function

$$F = (X+Z) (Y'+Z) (X'+Y+Z)$$

Being a POS expression, it is implemented in 2-levels as shown in the figure.

Introducing two successive inverters at the inputs of the AND gate results in the

By associating one of the inverters with the output of the first level OR gates and the other with the input of the AND gate, it is clear that this implementation is reducible to 2-level implementation where both levels are NOR gates as shown in Figure.

There are some other types of 2-level combinational circuits which are
- NAND-AND
- AND-NOR,
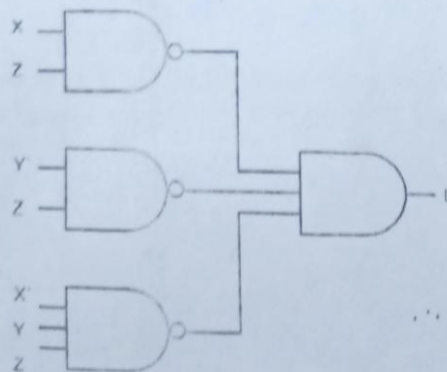- NOR-OR,
- OR-NAND

These are explained by examples.

AND-NOR functions:

Example 3: Implement the following function

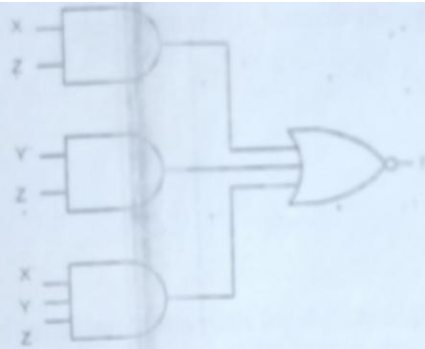$$F = \overline{XZ + \overline{Y}Z + \overline{X}YZ} \text{ or}$$
$$\overline{F} = XZ + \overline{Y}Z + \overline{X}YZ$$

Since F' is in SOP form, it can be implemented by using NAND-NAND circuit. By complementing the output we can get **F**, or by using *NAND-AND* circuit as shown in the figure.

It can also be implemented using *AND-NOR* circuit as it is equivalent to NAND-AND circuit as shown in the figure. (see animation in authorware version)
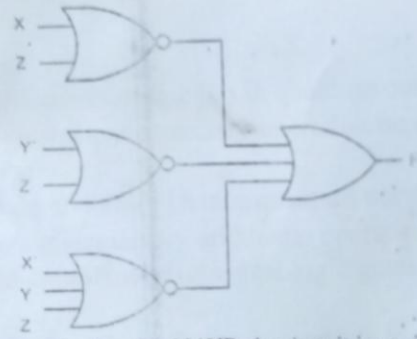
## OR-NAND functions:

Example 4: Implement the following function

$$F = \overline{(X+Z).(\overline{Y}+Z).(\overline{X}+Y+Z)} \text{ or}$$
$$\overline{F} = (X+Z)(\overline{Y}+Z)(\overline{X}+Y+Z)$$

Since F' is in POS form, it can be implemented by using NOR-NOR circuit. By complementing the output we can get F, or by using **NOR-OR** circuit as shown in the figure.

It can also be implemented using *OR-NAND* circuit as it is equivalent to NOR-OR circuit as shown in the figure. (see animation in authorware version)
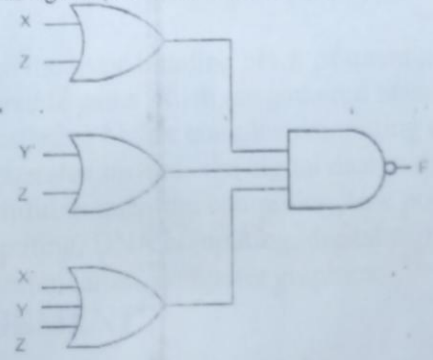
APPLICATIONS OF REVERSIBLE GATES

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require in energy efficiency, speed and performance .it include the area like

- Low power CMOS.
- Quantum computer.
- Nanotechnology.
- Optical computing.
- DNA computing.
- Computer graphics.
- Communication.
- Design of low power arithmetic and data path for digital signal processing (DSP).
- Field Programmable Gate Arrays (FPGAs) in CMOS technology.

The potential application areas of reversible computing include the following

- Nano computing
- Bio Molecular Computations
- Laptop/Handheld/Wearable Computers
- Spacecraft
- Implanted Medical Devices
- Wallet "smart cards"
- " Smart tags" on inventory
- Prominent application of reversible logic lies in quantum computers.
- Quantum gates perform an elementary unitary operation on one, two or more two–state quantum systems called qubits.
- Any unitary operation is reversible and hence quantum networks also.
- Quantum networks effecting elementary arithmetic operations cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).
- Thus, Quantum computers must be built from reversible logical components.

VI. CONCLUSION

The reversible circuits form the basic building block of quantum computers. This paper presents the primitive reversible gates which are gathered from literature and this paper helps researchers/designers in designing higher complex computing circuits using reversible gates. The paper can further be extended towards the digital design development using reversible logic circuits which are helpful in quantum computing, low power CMOS, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics.

VII. ACKNOWLEDGEMENTS

REFERENCES